CLEAN VERSION OF AMENDED SPECIFICATION PARAGRAPHS

MULTI-LAYER CHIP CAPACITOR
Applicant: Larry Eugene Mosley
Serial No.: 09/537,274

Paragraph beginning on page 4, line 6:

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Figure 2 illustrates a cross-section of a capacitor of one embodiment of the present invention. The capacitor 200 is fabricated on a substrate 202. Numerous layers of conductor 204 material separated by dielectric 208 are fabricated over the substrate. The conductive layers can be fabricated from any conductive material, such as but not limited to aluminum, copper or a metal alloy. The dielectric layers can be fabricated from any suitable dielectric, such as but not limited to $BaSrTiO_3$ (referred to herein as BST).

Paragraph beginning on page 4, line 23:

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The number and size of the vias can be selected to reduce resistance of the capacitor interconnects and allow for C4 mounting to a package. The vias can be connected together in one of three ways. The first interconnect method includes fabricating conducting interconnects on a top surface of the capacitor. These interconnects can be conductive strips that run perpendicular to the conductive strip layers. A second embodiment provides interconnects on a package, or circuit board. The vias, therefore, are each coupled to the interconnects on the package. In a third embodiment, some of the vias are coupled using interconnect lines on the capacitor and some of the vias are coupled using interconnect lines on the circuit board. Independent of how the vias are connected, lands (pads) can be made on the top of the capacitor to form C4 connections to attach to the package substrate.

Paragraph beginning on page 5, line 14:

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Referring to Figure 5, a cross-section of an alternate embodiment capacitor 300 is illustrated. While the embodiment of Figure 2 included strips of conductors that formed a pyramid-shaped cross-section, the present embodiment can be fabricated with full layers of conductors. The capacitor 300 includes a substrate 302. A first layer of conductor 304 is located

over the substrate. An second conductive layer 308 is separated from the first conductor by dielectric layer 306. Likewise dielectric layers 310 and 314 surround a third conductive layer 312. First electrical vias 316 are used to connect the first and third conductive layers 304, 312. A clearance is provided in layer 308 to isolate the first electrical vias 316 from the second conductive layer 308. Second electrical vias 318 contact the second conductive layer 308. Clearance areas are provided in the first conductive layer 304 to isolate the second electrical vias 318 from the first conductive layer 304. C4 lands 320 can be provided to allow the capacitor 300 to be mounted to a circuit board. In this embodiment the conductive layers do not decrease in surface area as the number of layers increase.

Paragraph beginning on page 6, line 1:

In another embodiment illustrated in Figure 6, the conductive layers are fabricated as described with reference to Figure 2. In this embodiment, however, the interconnect vias pass through the second conductive layer to connect the first and third conductive layers using common vias. Again, a clearance area needs to be provided in the intermediate conductor to avoid shorts between the alternate conductor layers.

Paragraph beginning on page 6, line 12:

Figure 7 illustrates a cross section of an embedded capacitor embodiment comprising a capacitor 400 that is physically coupled to a dielectric layer 402. In one embodiment, the capacitor is attached to the dielectric using an adhesive. Vias 404 are then formed through the dielectric layer to expose electrical connections on the capacitor. The vias are then plated with a conductor to form an electrical interconnect to the capacitor. This embodiment, therefore, provides an alternate manner of coupling the capacitor to a circuit. Figure 8 illustrates another embodiment of the present invention where electrical vias 410 are formed through the substrate 402 of the capacitor 400. The capacitor can be fabricated as explained herein, but with the

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additional electrical vias 410. These vias 410 allow circuits to be coupled to both sides of the capacitor and provided a more direct conductive path between the circuits.

Paragraph beginning on page 6, line 23:

Figure 9 illustrates an embedded capacitor package 500. The capacitor 480 includes interconnect lands on each side of the capacitor and can be fabricated as illustrated in Figure 8. The capacitor has a first circuit package 450 formed on the top of the capacitor and a second package circuit 460 formed on the bottom of the capacitor. The packages have at least one conductive layer 440 and dielectric layers. The conductive layers are coupled using vias 404. These vias can be formed using a laser and plating the opening created with the laser. Other techniques can be used to fabricate and connect the package layers. The embodiment of Figure 9, therefore, illustrates that the capacitor can be embedded in a multi-layer circuit package.

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Clean Version of Pending Claims

MULTI-LAYER CHIP CAPACITOR
Applicant: Larry Eugene Mosley
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1. (Once Amended) A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over the substrate;

a first insulator layer located over the first conductive layer;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductor layer; and

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductor layers.

2. The multi layer integrated circuit capacitor of claim 1 further comprising a plurality of controlled collapse chip connection (C4) lands fabricated on the third insulator layer and in electrical contact with the plurality of conductive vias.

3. The multi layer integrated circuit capacitor of claim 2 wherein the C4 lands are fabricated in staggered columns in a plan view.

4. (Once Amended) The multi layer integrated circuit capacitor of claim 1 wherein at least one of the conductive layers comprise a metal material and at least one of the insulator layers comprise $BaSrTiO_3$.

5. (Once Amended) The multi layer integrated circuit capacitor of claim 4 wherein at least one of the conductive layers are fabricated from a copper.

C1 Cont.

6. (Once Amended) The multi layer integrated circuit capacitor of claim 1 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer being patterned to form interconnect lines that selectively connect the plurality of conductive vias.

7. The multi layer integrated circuit capacitor of claim 1 wherein the second and third conductive layers are fabricated in a plurality of strips, such that a surface area of the second conductive layer is less than a surface area of the first conductive layer and a surface area of the third conductive layer is less than the surface area of the second conductive layer.

C1 Cont.

8. The multi layer integrated circuit capacitor of claim 1 wherein some of the plurality of conductive vias pass through the second conductive layer without forming an electrical connection with the second conductive layer.

9. (Once Amended) A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over the substrate;

a first insulator layer located over the first conductive layer;

a second conductive layer located over the first insulator layer, the second conductive layer being fabricated as a plurality of laterally spaced strips such that a surface area of the second conductive layer is less than a surface area of the first conductive layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer, the third conductive layer being fabricated as a plurality of laterally spaced strips such that a surface area of the third conductive layer is less than the surface area of the second conductive layer;

a third insulator layer located over the third conductive layer;

a first plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the third conductive layer;

a second plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the second conductive layer; and

a third plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first conductive layer.

10. (Once Amended) The multi layer integrated circuit capacitor of claim 9 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer being patterned to form interconnect lines that selectively connect at least one of the pluralities of conductive vias.

11. (Once Amended) A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over the substrate;

a first insulator layer located over the first conductive layer;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductive layer;

a first plurality of conductive vias downwardly extending through the third insulator layer, the third conductive layer, the second insulator layer, the second conductive layer and the first insulator layer to provide electrical interconnection to the first and third conductive layers; and

a second plurality of conductive vias downwardly extending through the third insulator layer, the third conductive layer, and the second insulator layer to provide electrical interconnection to the second conductive layer.

12. (Once Amended) The multi layer integrated circuit capacitor of claim 11 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive

layer being patterned to form interconnect lines that selectively connect at least one of the pluralities of conductive vias.

13. (Once Amended) The multi layer integrated circuit capacitor of claim 11 wherein at least one of the conductive layers comprise a metal material and wherein at least one of the insulator layers comprise $BaSrTiO_3$.

14. (Once Amended) A circuit board assembly comprising:

a circuit board having a pair of supply voltage interconnect lines;

a first integrated circuit die mounted on the circuit board and electrically connected to the supply voltage interconnect lines; and

a second integrated circuit die mounted on the circuit board and electrically connected to the supply voltage interconnect lines, the second integrated circuit package comprising a capacitor having:

a substrate;

a first conductive layer located over the substrate;

a first insulator layer located over the first conductive layer;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductive layer; and

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductive layers.

15. The circuit board assembly of claim 14 wherein the second integrated circuit package comprises a plurality of controlled collapse chip connection (C4) lands that are electrically connected to the plurality of conductive vias and the supply voltage interconnect lines.

16. The circuit board assembly of claim 14 wherein the first integrated circuit package is a processor circuit.

17. (Once Amended) The circuit board assembly of claim 14 wherein at least one of the conductive layers comprise a metal material and wherein at least one of the insulator layers comprise $BaSrTiO_3$.

18. (Once Amended) The circuit board assembly of claim 14 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer being patterned to form interconnect lines that selectively connect the plurality of plurality of conductive vias.

19. (Once Amended) A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over the substrate;

a first insulator layer located over the first conductive layer;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductive layer; and

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first, second, and third conductive layers, the plurality of conductive vias further extending through the substrate to provide electrical interconnection to both a top surface and a bottom surface of the integrated circuit capacitor.

20. (Once Amended) The multi layer integrated circuit capacitor of claim 19 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive

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layer being patterned to form interconnect lines that selectively connect the plurality of conductive vias.

21. (Once Amended) The multi layer integrated circuit capacitor of claim 1 wherein each of the conductor layers comprise a metal material and wherein each of the insulator layers comprise $BaSrTiO_3$.